



## GENERAL DESCRIPTION



The ICS87931I is a low voltage, low skew LVC MOS/LVTTL Clock Multiplier/Zero Delay Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. With output frequencies up to 150MHz, the ICS87931I is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS87931I contains frequency configurable outputs and an external feedback input for regenerating clocks with “zero delay”.

Selectable clock inputs, CLK1 and differential CLK0, nCLK0 support redundant clock applications. The CLK\_SEL input determines which reference clock is used. The output divider values of Bank A, B and C are controlled by the DIV\_SELA, DIV\_SELB and DIV\_SELC, respectively.

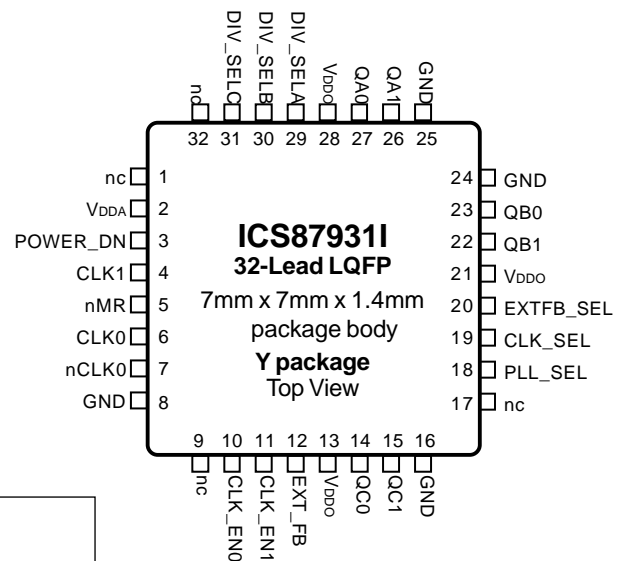
For test and system debug purposes, the PLL\_SEL input allows the PLL to be bypassed. When LOW, the nMR input resets the internal dividers and forces the outputs to the high impedance state.

The effective fanout of the ICS87931I can be increased to 12 by utilizing the ability of each output to drive two series terminated transmission lines.

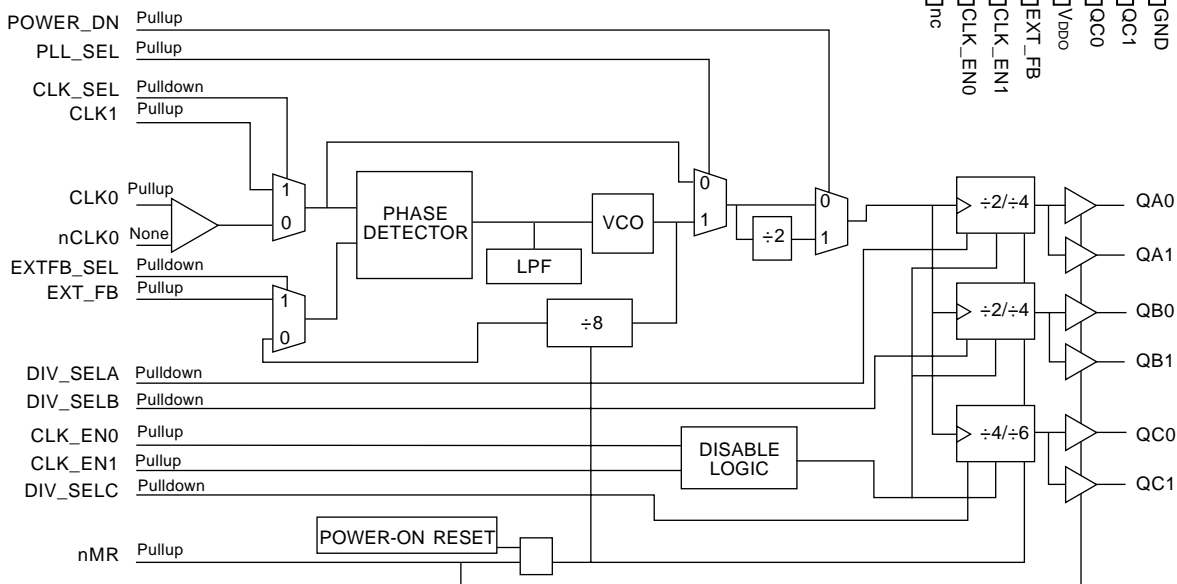
## FEATURES

- Fully integrated PLL
- 6 LVC MOS/LVTTL outputs, 7Ω typical output impedance
- Selectable differential CLK0, nCLK0 or LVC MOS/LVTTL clock for redundant clock applications
- Maximum output frequency: 150MHz
- VCO range: 220MHz to 480MHz
- External feedback for “zero delay” clock regeneration
- Output skew, Same Frequency: 300ps (maximum)
- Output skew, Different Frequency: 400ps (maximum)
- Cycle-to-cycle jitter: 100ps (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible with MPC931

## PIN ASSIGNMENT



## BLOCK DIAGRAM





**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 9, 17, 32	nc	Unused		No connect.
2	V <sub>DDA</sub>	Power		Analog supply pin.
3	POWER_DN	Input	Pullup	Controls the frequency being fed to the output dividers. LVCMOS / LVTTL interface levels.
4	CLK1	Input	Pullup	Clock input. LVCMOS / LVTTL interface levels.
5	nMR	Input	Pullup	Active LOW Master reset. When logic LOW, the internal dividers are reset causing the outputs to go low. When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
6	CLK0	Input	Pullup	Non-inverting differential clock input.
7	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating.
8, 16, 24,25	GND	Power		Power supply ground.
10, 11	CLK_EN0, CLK_EN1	Input	Pullup	Controls the enabling and disabling of the clock outputs. See Table 3B. LVCMOS / LVTTL interface levels.
12	EXT_FB	Input	Pullup	External feedback. When LOW, selects internal feedback. When HIGH, selects EXT_FB. LVCMOS / LVTTL interface levels.
13, 21, 28	V <sub>DDO</sub>	Power		Output supply pins.
14, 15	QC0, QC1	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
18	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL. LVCMOS / LVTTL interface levels.
19	CLK_SEL	Input	Pulldown	Clock select input. Selects the Phase Detector Reference. When LOW, selects CLK0, nCLK0. When HIGH, selects CLK1. LVCMOS / LVTTL interface levels.
20	EXTFB_SEL	Input	Pulldown	External feedback select. LVCMOS / LVTTL interface levels.
22, 23	QB1, QB0	Output		Bank B clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
26, 27	QA1, QA0	Output		Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
29	DIV_SELA	Input	Pulldown	Determines output divider values for Bank A as described in Table 4A. LVCMOS / LVTTL interface levels.
30	DIV_SELB	Input	Pulldown	Determines output divider values for Bank B as described in Table 4A. LVCMOS / LVTTL interface levels.
31	DIV_SELC	Input	Pulldown	Determines output divider values for Bank C as described in Table 4A. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DDA</sub> , V <sub>DDO</sub> = 3.465V		12		pF
R <sub>OUT</sub>	Output Impedance			7		Ω



**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs		Function	
Control Pin	Logic 0	Logic 1	
CLK_SEL	CLK0, nCLK0	CLK1	
PLL_SEL	Bypass PLL	PLL Enabled	
EXTFB_SEL	Internal Feedback	EXT_FB	
POWER_DN	VCO/1	VCO/2	
nMR	Master Reset/Output Hi Z	Enable Outputs	
DIV_SELA:DIV_SELCA	QA(÷2); QB(÷2); QC(÷4)	QA(÷4); QB(÷4); QC(÷6)	

**TABLE 3B. CLK\_ENx FUNCTION TABLE**

Inputs				
CLK_EN1	CLK_EN0	DIV_SELA:DIVSELCA		
		QAx	QBx	QCx
0	0	Toggle	LOW	LOW
0	1	LOW	LOW	Toggle
1	0	Toggle	LOW	Toggle
1	1	Toggle	Toggle	Toggle

**TABLE 4A. VCO FREQUENCY FUNCTION TABLE**

Inputs			Outputs					
DIV_SELA	DIV_SELCA	DIV_SELCA	QAx		QBx		QCx	
			POWER_DN = 0	POWER_DN = 1	POWER_DN = 0	POWER_DN = 1	POWER_DN = 0	POWER_DN = 1
0	0	0	VCO/2	VCO/4	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	VCO/2	VCO/4	VCO/2	VCO/4	VCO/6	VCO/12
0	1	0	VCO/2	VCO/4	VCO/4	VCO/8	VCO/4	VCO/8
0	1	1	VCO/2	VCO/4	VCO/4	VCO/8	VCO/6	VCO/12
1	0	0	VCO/4	VCO/8	VCO/2	VCO/4	VCO/4	VCO/8
1	0	1	VCO/4	VCO/8	VCO/2	VCO/4	VCO/6	VCO/12
1	1	0	VCO/4	VCO/8	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	VCO/4	VCO/8	VCO/4	VCO/8	VCO/6	VCO/12

**TABLE 4B. INPUT REFERENCE FREQUENCY TO OUTPUT FREQUENCY FUNCTION TABLE (INTERNAL FEEDBACK ONLY)**

Inputs			Outputs					
DIV_SELA	DIV_SELCA	DIV_SELCA	QAx		QBx		QCx	
			POWER_DN = 0	POWER_DN = 1	POWER_DN = 0	POWER_DN = 1	POWER_DN = 0	POWER_DN = 1
0	0	0	4x	2x	4x	2x	2x	x
0	0	1	4x	2x	4x	2x	4/3x	2/3x
0	1	0	4x	2x	2x	x	2x	x
0	1	1	4x	2x	2x	x	4/3x	2/3x
1	0	0	2x	x	4x	2x	2x	x
1	0	1	2x	x	4x	2x	4/3x	2/3x
1	1	0	2x	x	2x	x	2x	x
1	1	1	2x	x	2x	x	4/3x	2/3x

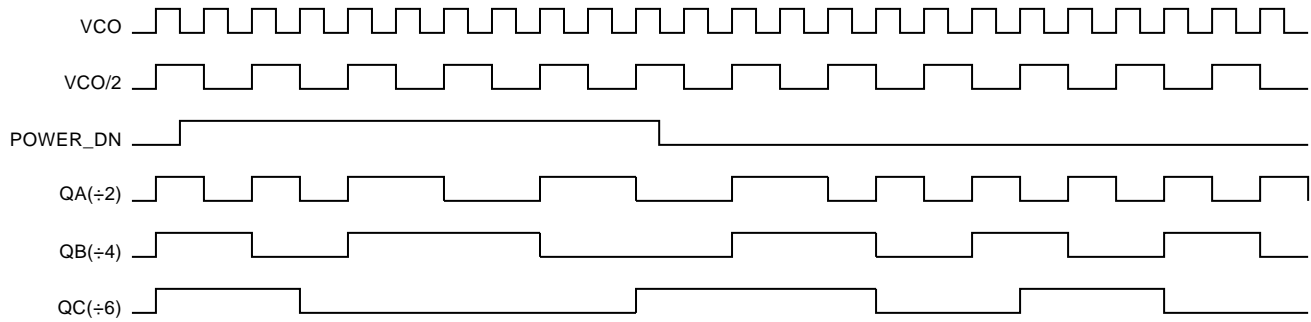


FIGURE 1A. POWER\_DN TIMING DIAGRAM

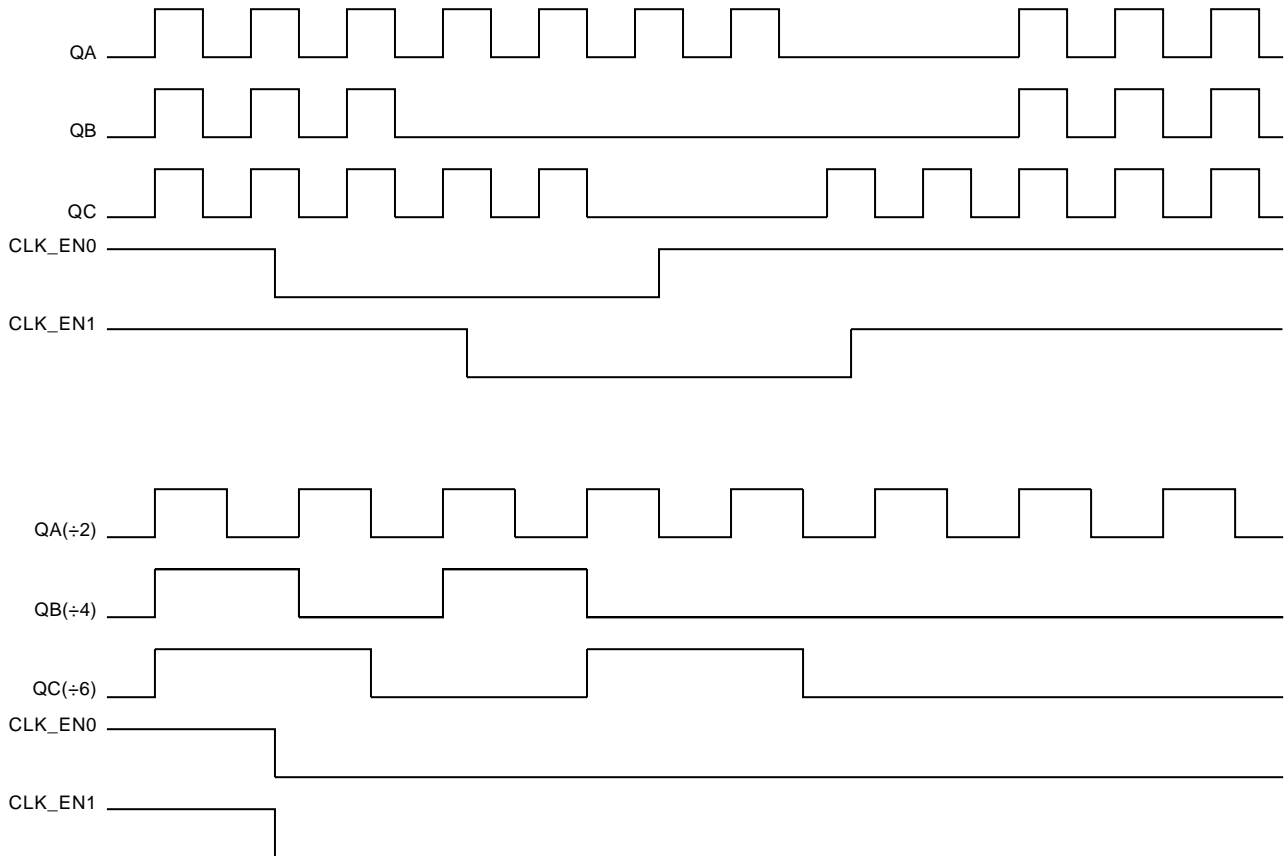


FIGURE 1B. CLK\_ENx TIMING DIAGRAMS



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_i$	-0.5V to $V_{DDA} + 0.5V$
Outputs, $V_o$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 5A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DDA}$	Analog Supply Current			20		mA
$I_{DDO}$	Output Supply Current			100		mA

**TABLE 5B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	DIV_SELA:DIV_SEL, CLK_EN0, CLK_EN1, POWER_DN, nMR, CLK_SEL, PLL_SEL, EXTFB_SEL	2		$V_{DD} + 0.3$	V
		CLK1, EXT_FB	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	DIV_SELA:DIV_SEL, CLK_EN0, CLK_EN1, POWER_DN, nMR, CLK_SEL, PLL_SEL, EXTFB_SEL	-0.3		0.8	V
		CLK1, EXT_FB	-0.3		1.3	V
$I_{IN}$	Input Current				$\pm 120$	$\mu A$
$V_{OH}$	Output High Voltage; NOTE 1	$I_{OH} = -20mA$	2.4			V
$V_{OL}$	Output Low Voltage; NOTE 1	$I_{OL} = 20mA$			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, 3.3V Output Load Test Circuit.

**TABLE 5C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IN}$	Input Current				$\pm 120$	$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is  $V_{DDA} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	Input Reference Frequency NOTE: Input reference frequency is limited by the divider selection and the VCO lock range.				150	MHz

**TABLE 7. AC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{MAX}$	Output Frequency	QAx, QBx	$\div 2$		150	MHz	
		QAx, QBx, QCx	$\div 4$		120	MHz	
		QCx	$\div 6$		80	MHz	
$t_{PD}$	Propagation Delay; NOTE 1	CLK1 to EXT_FB	fref = 50MHz, FB = $\div 8$	-375	-200	-50	ps
		CLK0, nCLK0 to EXT_FB		-100	50	200	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 4	Same Frequency			300	ps	
		Different Frequency			400	ps	
$f_{jitter(cc)}$	Cycle-to-Cycle Jitter; NOTE 4				100	ps	
$f_{VCO}$	PLL VCO Lock Range		220		480	MHz	
$t_R/t_F$	Output Rise Time; NOTE 3	0.8V to 2.0V	0.1		1	ns	
odc	Output Duty Cycle		45		55	%	
$t_{LOCK}$	PLL Lock Time				10	ms	
$t_{PZL}, t_{PZH}$	Output Enable Time; NOTE 3		2		10	ns	
$t_{PLZ}, t_{PHZ}$	Output Disable Time; NOTE 3		2		8	ns	

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to  $V_{DDO}/2$  of the output

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

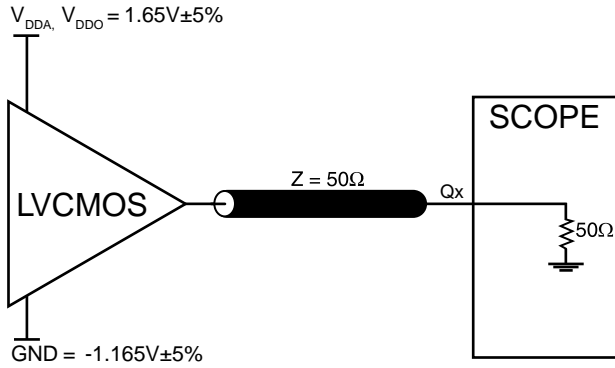
Measured at  $V_{DDO}/2$ .

NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

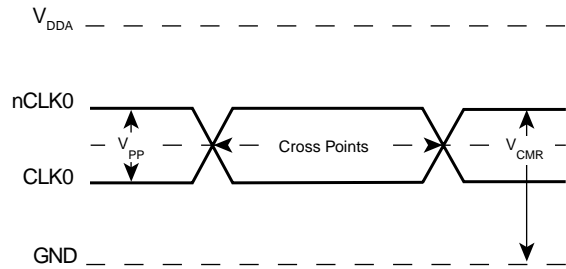
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



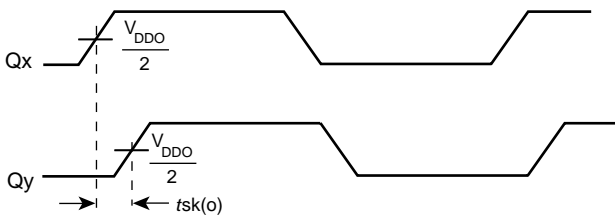
## PARAMETER MEASUREMENT INFORMATION



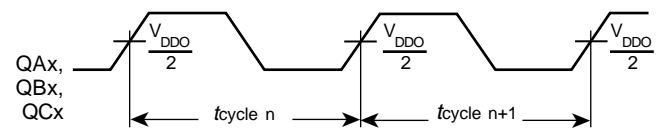
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



**DIFFERENTIAL INPUT LEVEL**



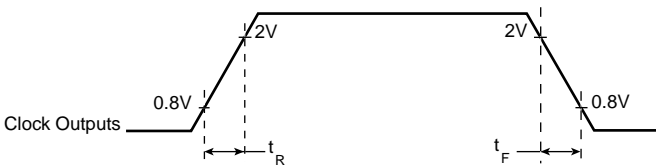
**OUTPUT SKEW**



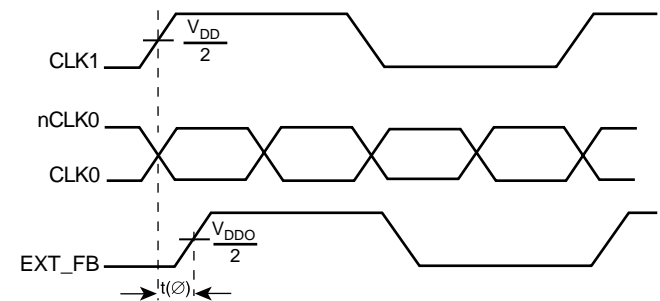
$$t_{jit(cc)} = t_{cycle n} - t_{cycle n+1}$$

1000 Cycles

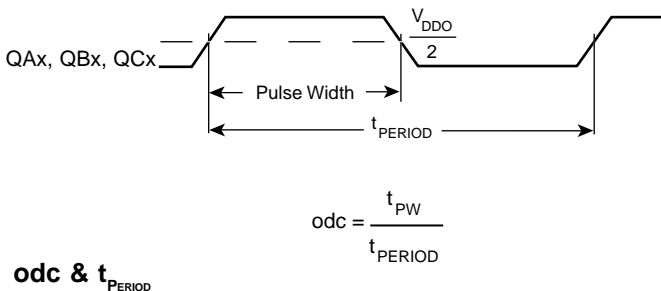
**CYCLE-TO-CYCLE JITTER**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



**odc &  $t_{PERIOD}$**



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

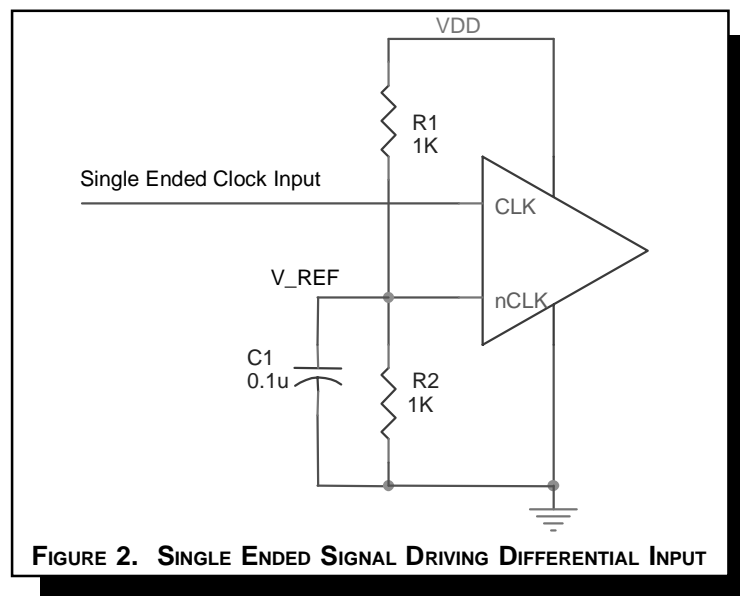


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

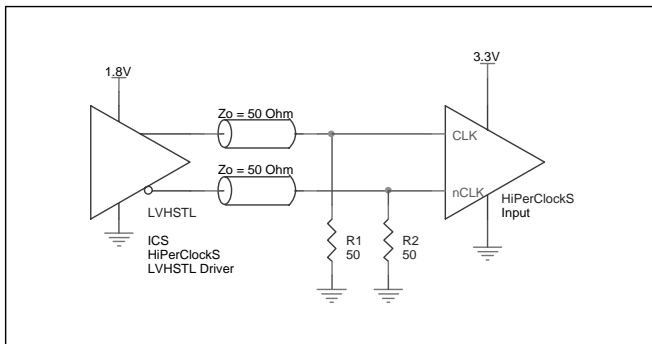




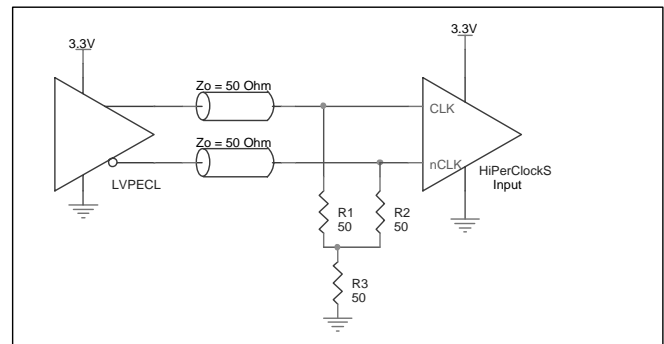
#### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

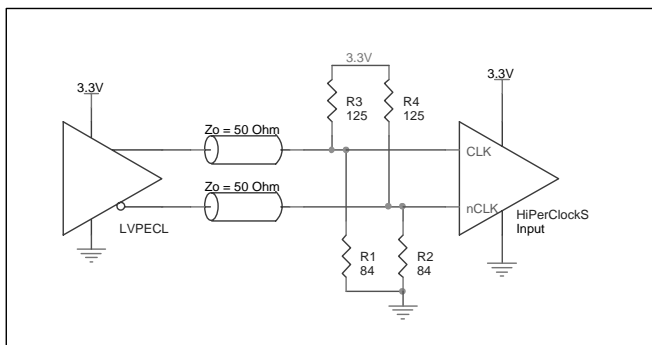
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



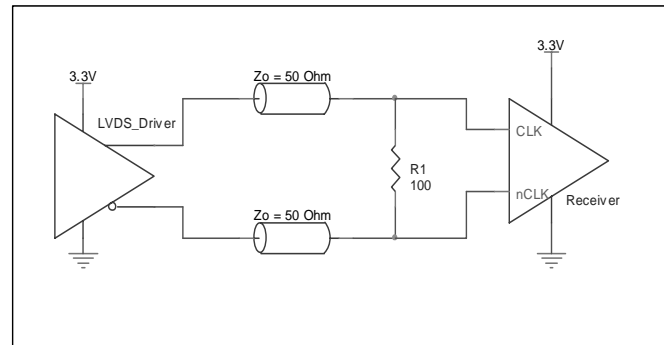
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



## SCHEMATIC EXAMPLE

Figure 4A shows a schematic example of using an ICS87931I. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible

to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the  $V_{DDA}$  pin as possible.

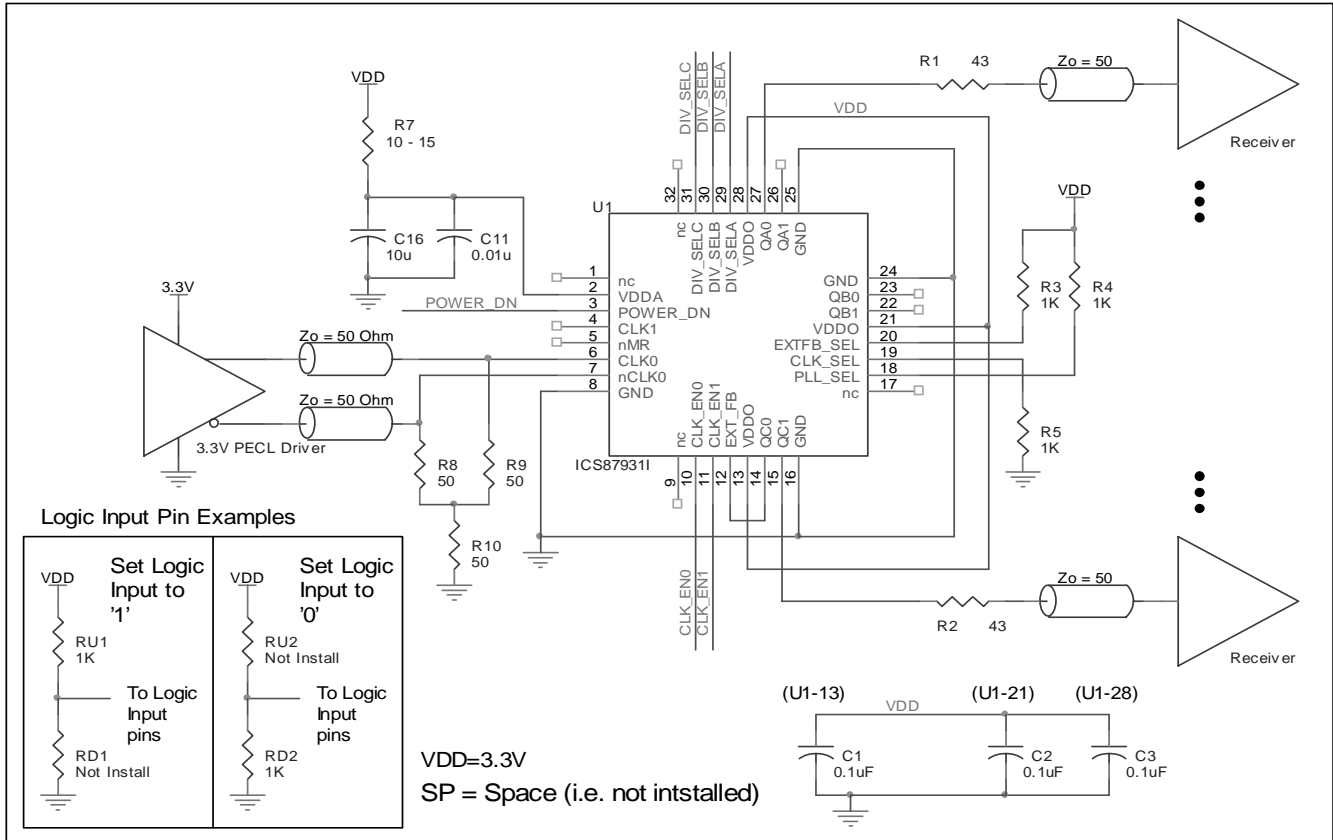


FIGURE 4A. ICS87931I SCHEMATIC EXAMPLE



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

### POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the  $V_{DDA}$  pin as possible.

### CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the

trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

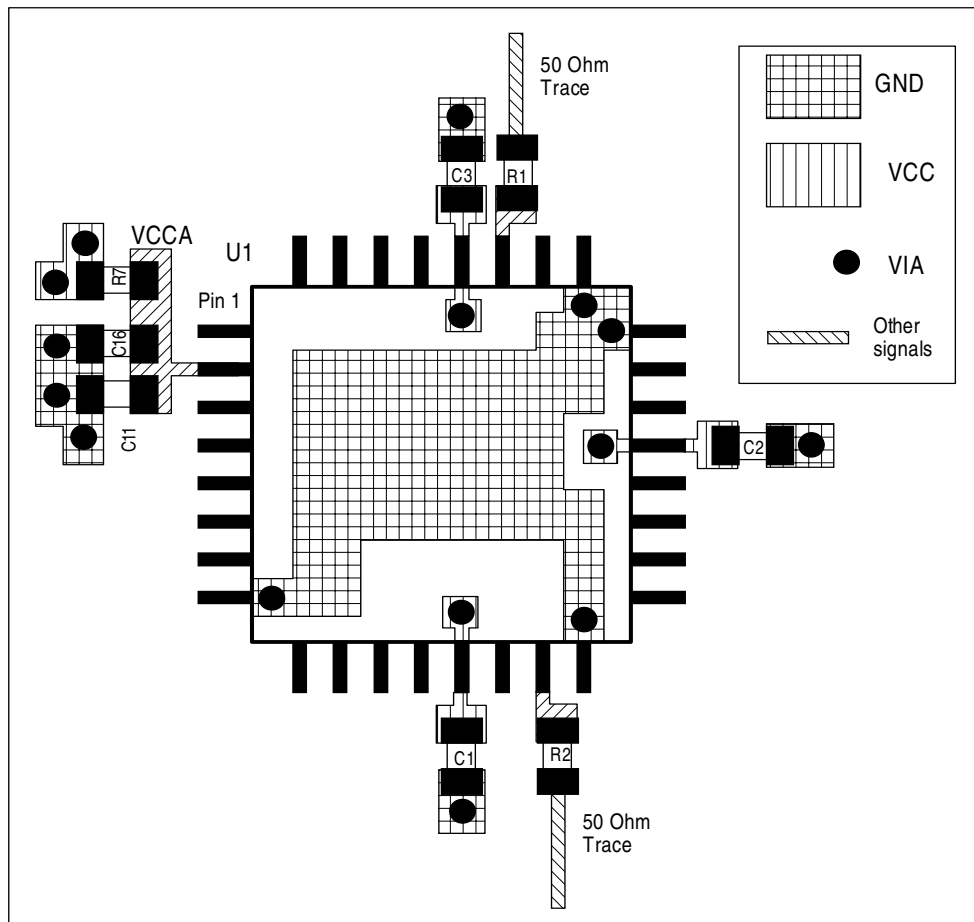


FIGURE 4B. PCB BOARD LAYOUT FOR ICS87931I



## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS87931I is: 2942



PACKAGE OUTLINE - Y SUFFIX

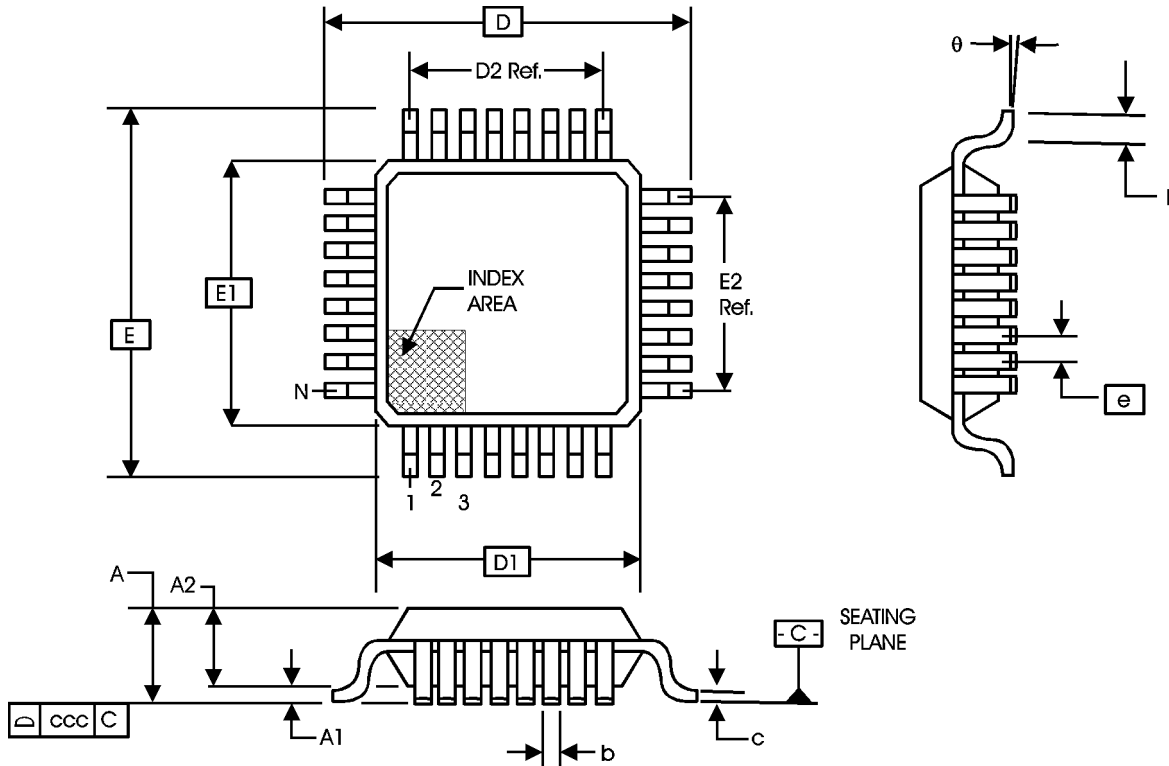


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

**ICS87931I**  
LOW SKEW, 1-TO-6  
LVCMOS/LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

**TABLE 10. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS87931BYI	ICS87931BI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS87931BYIT	ICS87931BI	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

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